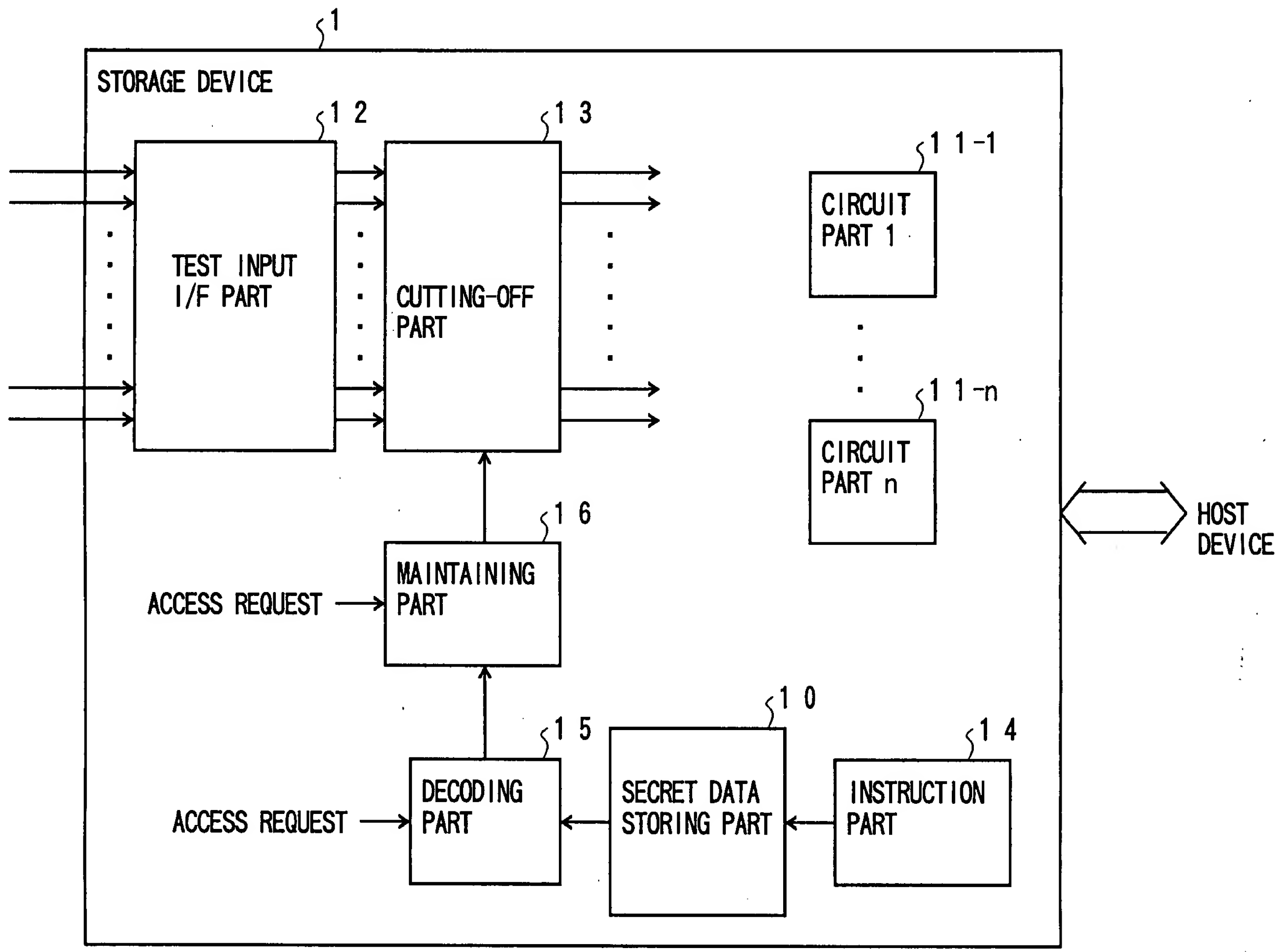
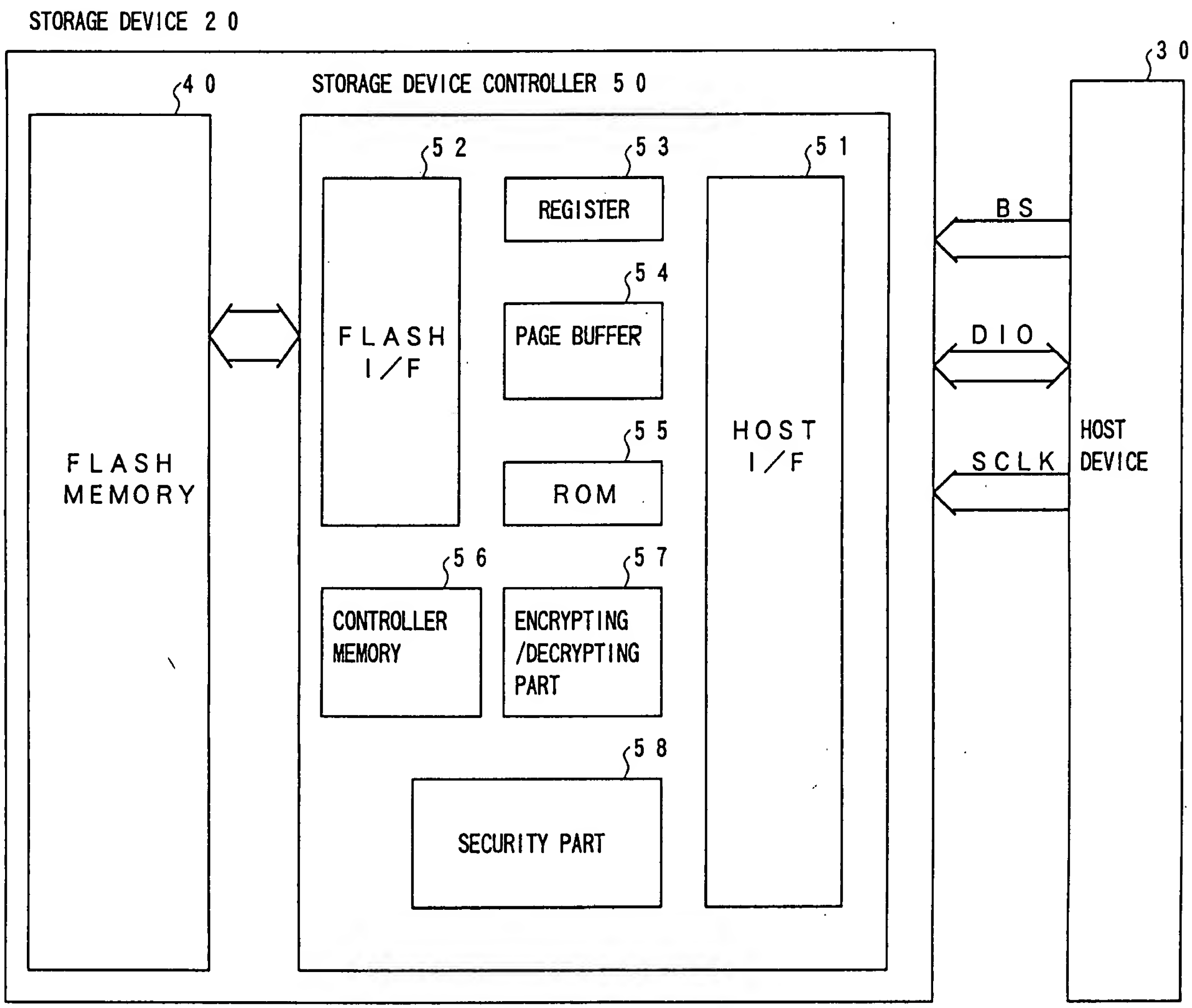
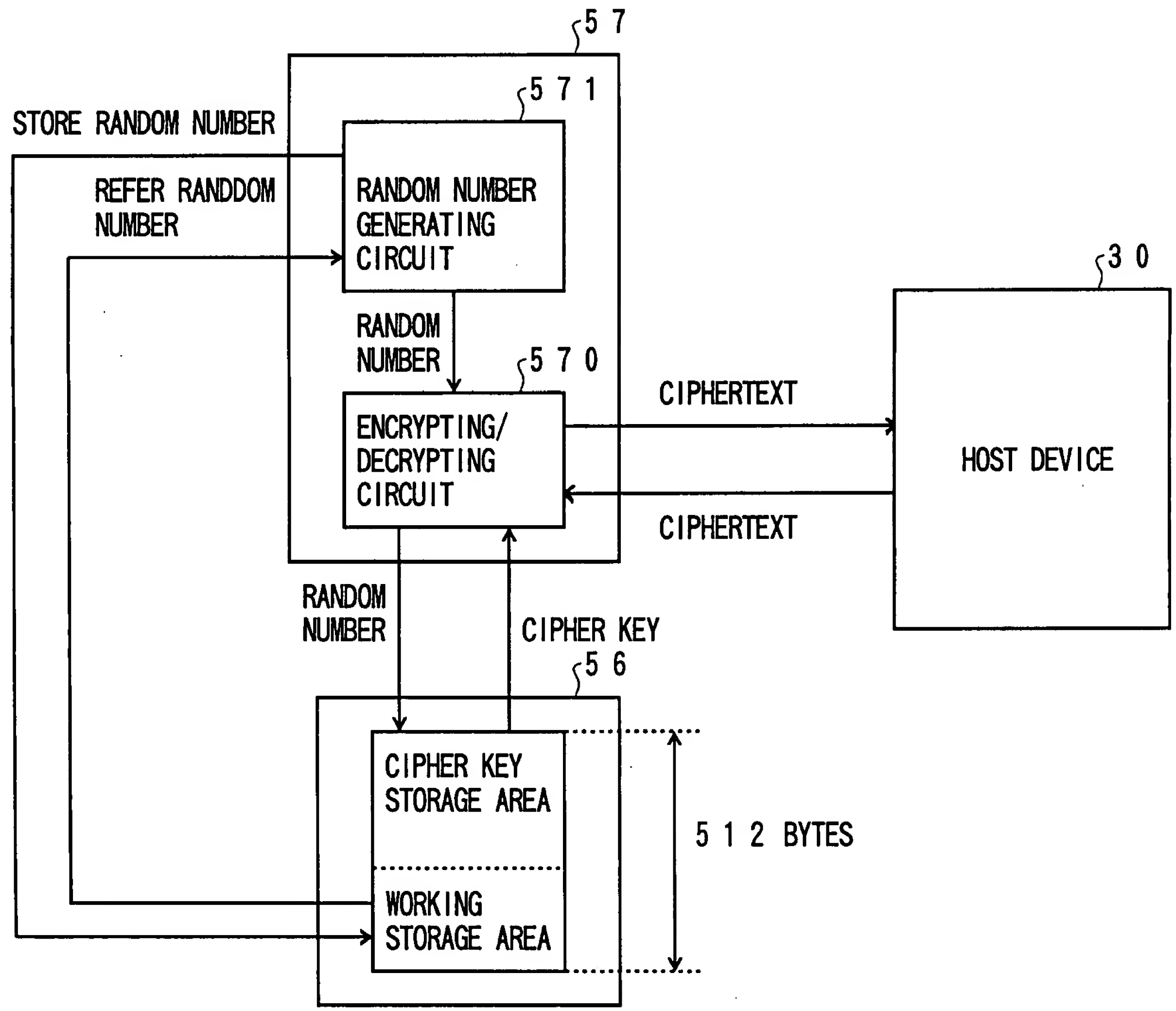
F I G. 1



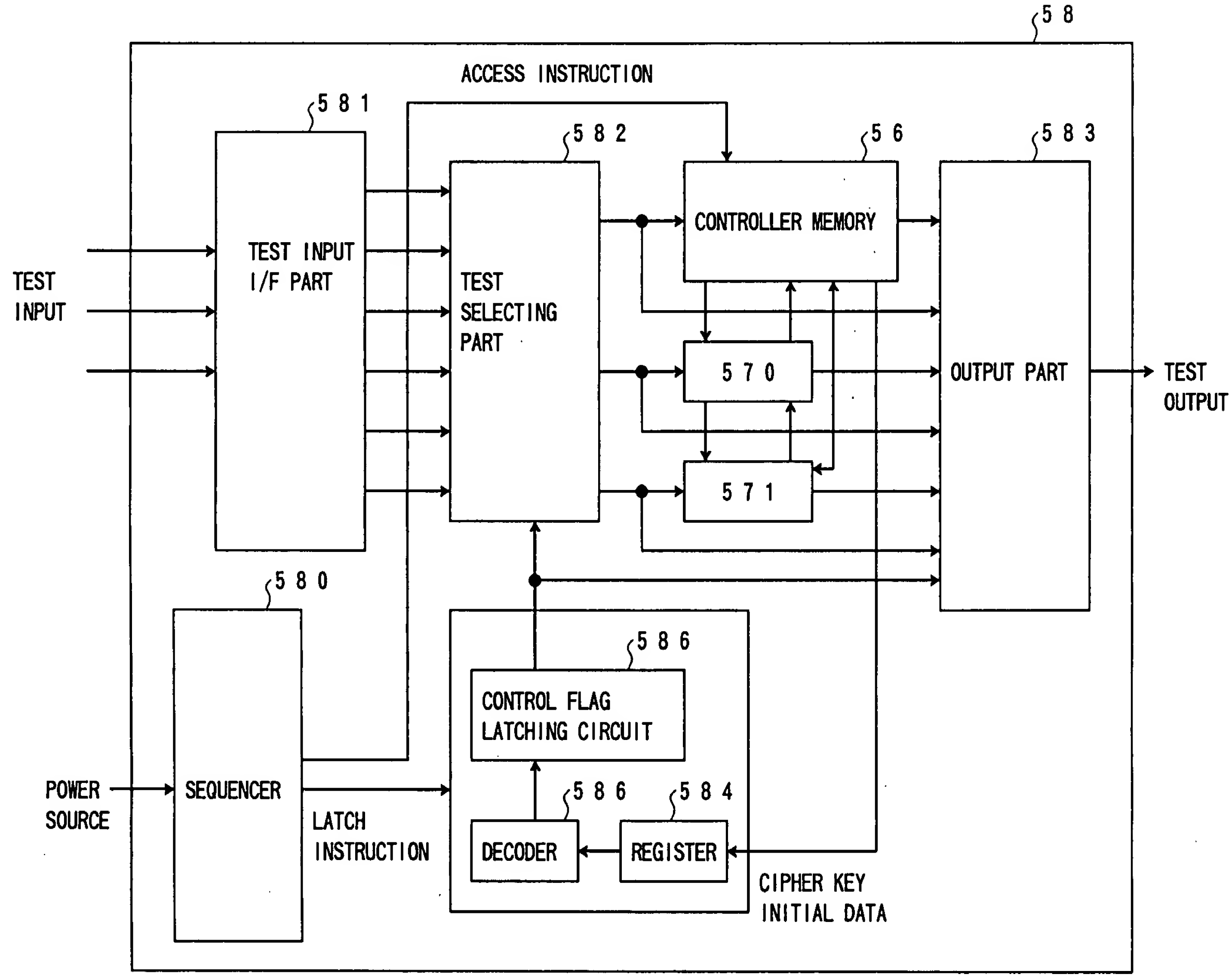
F I G. 2


STORAGE DEVICE 2 0
4 0
FLASH MEMORY
STORAGE DEVICE CONTROLLER 5 0
5 2
FLASH I/F
5 3
REGISTER
5 4
PAGE BUFFER
5 5
ROM
5 6
CONTROLLER MEMORY
5 7
ENCRYPTING /DECRYPTING PART
5 8
SECURITY PART
5 1
HOST I/F
BS
DIO
SCLK
3 0
HOST DEVICE

F I G. 3

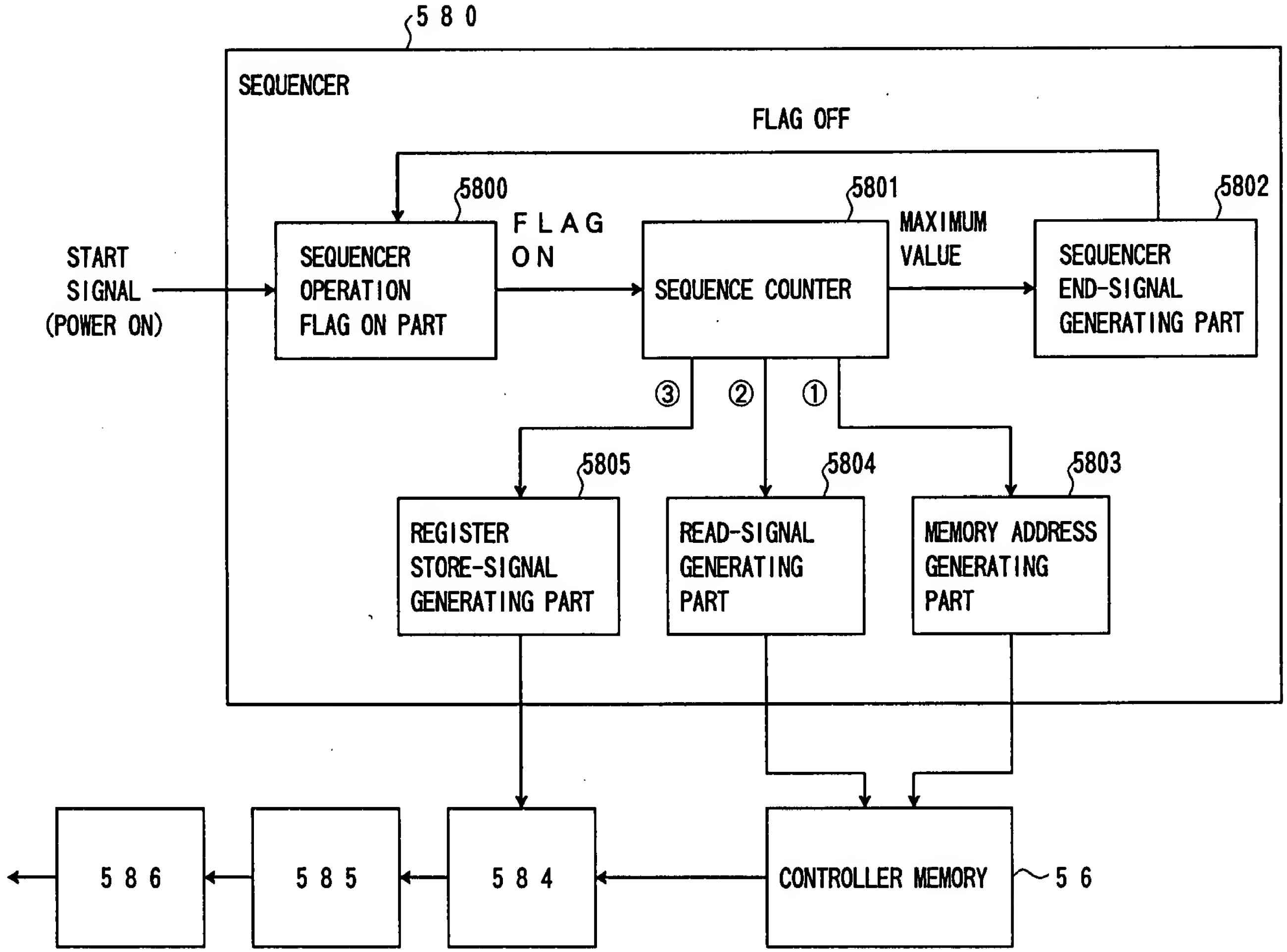

5 7
5 7 1
STORE RANDOM NUMBER
REFER RANDDOM NUMBER
RANDOM NUMBER GENERATING CIRCUIT
RANDOM NUMBER
5 7 0
ENCRYPTING/ DECRYPTING CIRCUIT
CIPHERTEXT
CIPHERTEXT
3 0
HOST DEVICE
RANDOM NUMBER
CIPHER KEY
5 6
CIPHER KEY STORAGE AREA
WORKING STORAGE AREA
5 1 2 BYTES

F I G. 4



5 8
ACCESS INSTRUCTION
5 8 1
TEST INPUT
I/F PART
5 8 2
TEST
SELECTING
PART
5 6
CONTROLLER MEMORY
5 8 3
OUTPUT PART
5 7 0
5 7 1
TEST
INPUT
TEST
OUTPUT
5 8 0
SEQUENCER
POWER
SOURCE
LATCH
INSTRUCTION
5 8 6
CONTROL FLAG
LATCHING CIRCUIT
5 8 6
DECODER
5 8 4
REGISTER
CIPHER KEY
INITIAL DATA

F I G. 5



5 8 0
SEQUENCER
FLAG OFF
START SIGNAL (POWER ON)
5800
SEQUENCER OPERATION FLAG ON PART
FLAG ON
5801
SEQUENCE COUNTER
MAXIMUM VALUE
5802
SEQUENCER END-SIGNAL GENERATING PART
③
②
①
5805
REGISTER STORE-SIGNAL GENERATING PART
5804
READ-SIGNAL GENERATING PART
5803
MEMORY ADDRESS GENERATING PART
5 8 6
5 8 5
5 8 4
CONTROLLER MEMORY
5 6

FIG. 6

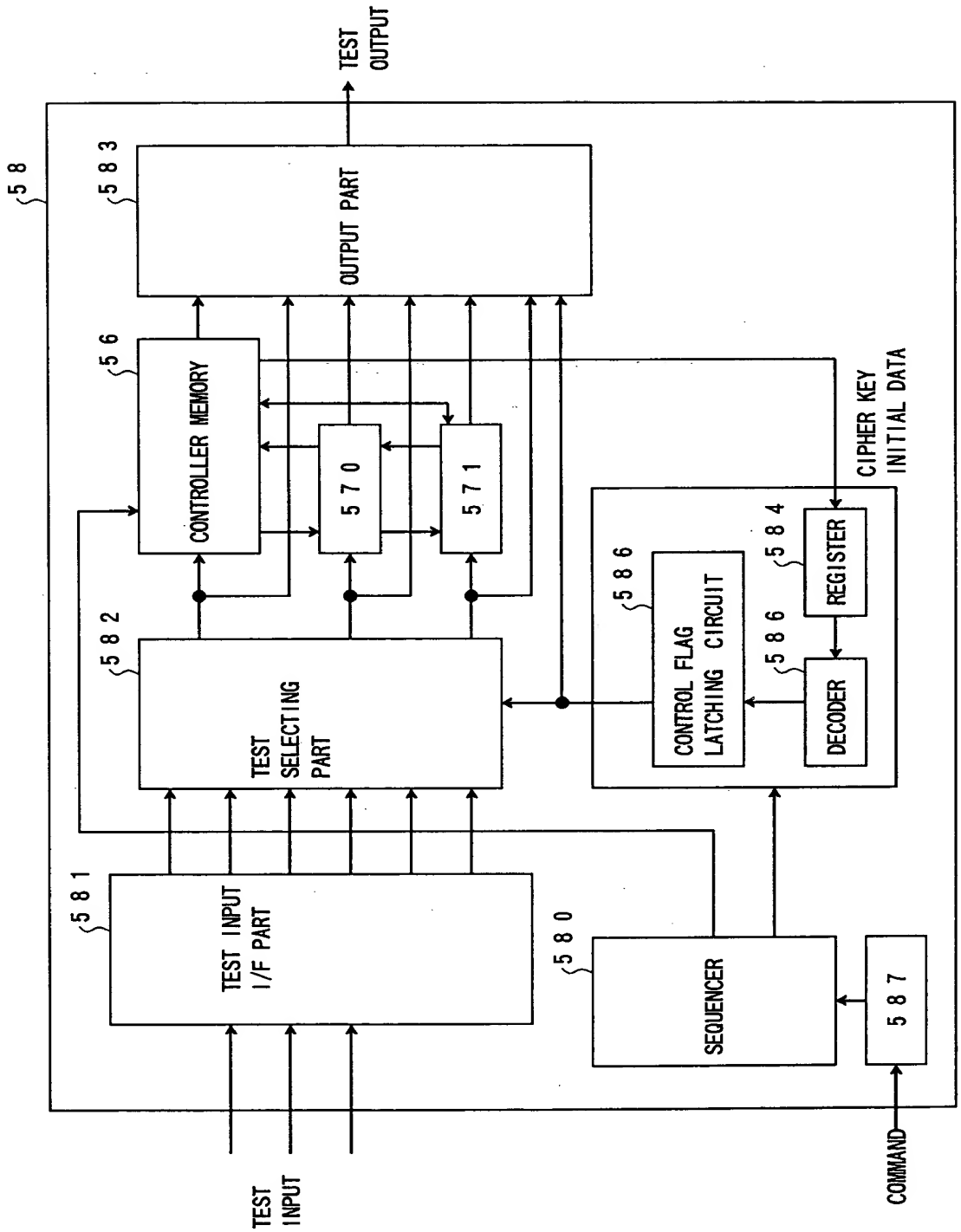
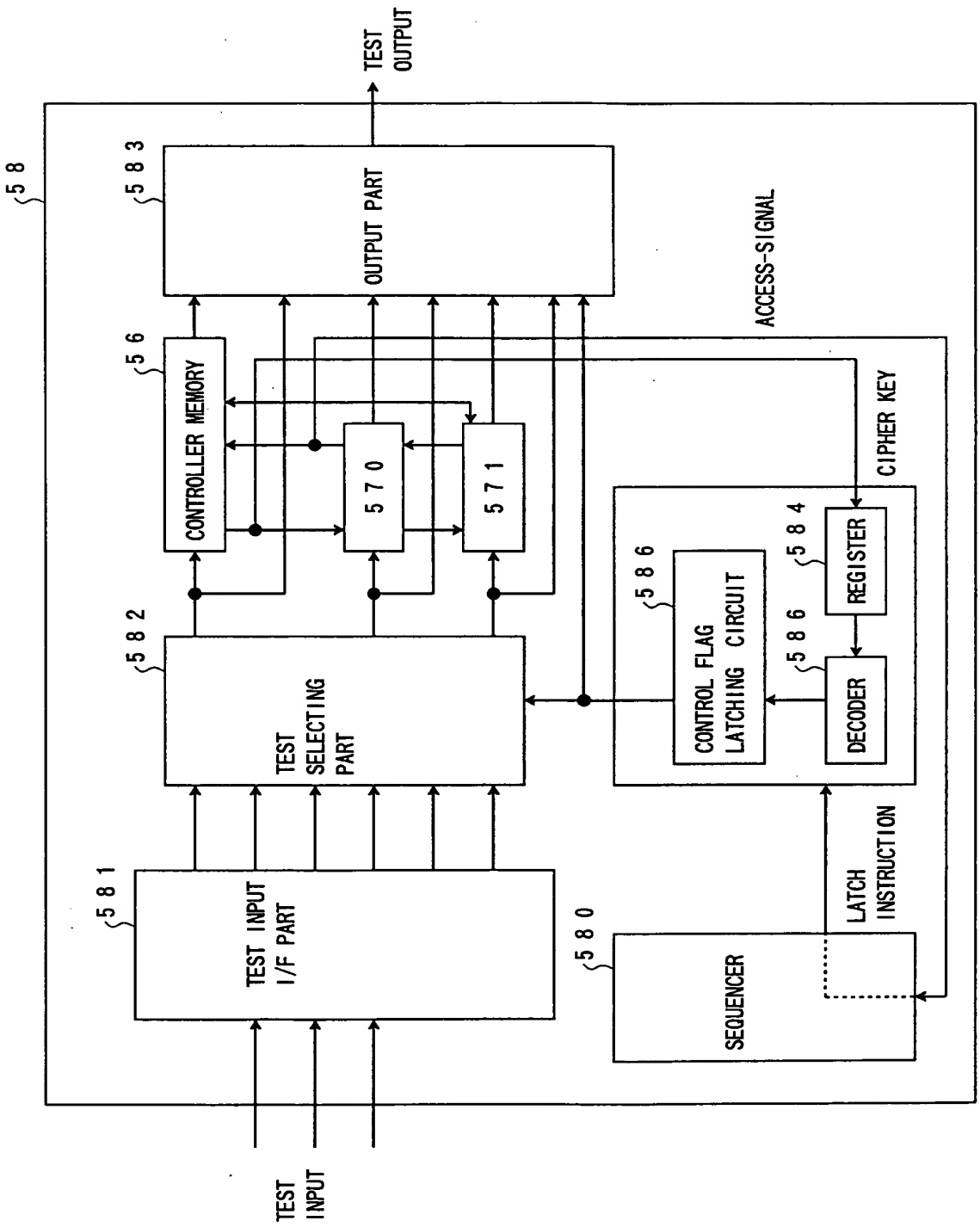
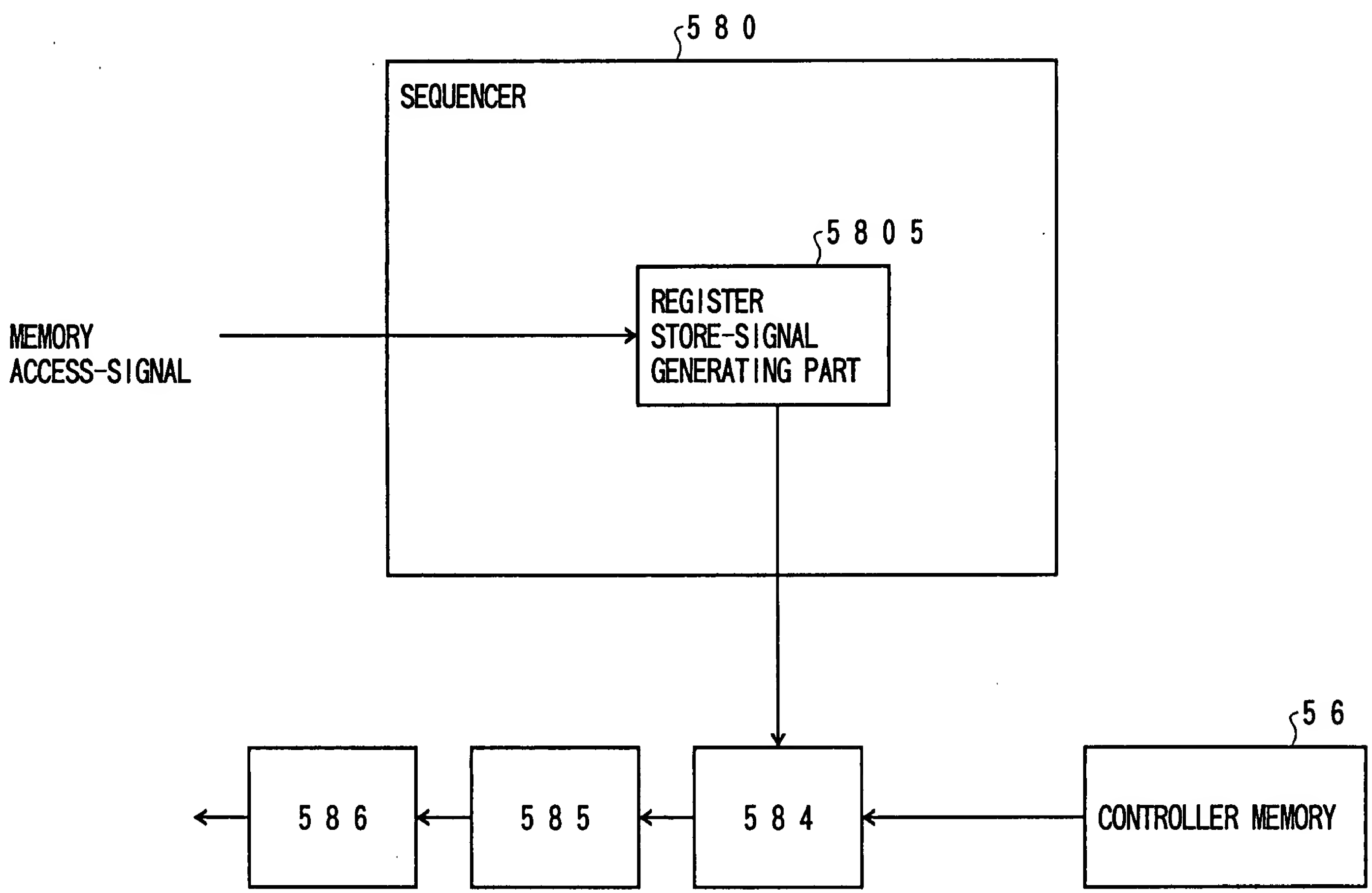

58
583
OUTPUT PART
TEST OUTPUT
56
CONTROLLER MEMORY
570
571
582
TEST SELECTING PART
586
CONTROL FLAG LATCHING CIRCUIT
584
REGISTER
586
DECODER
CIPHER KEY INITIAL DATA
581
TEST INPUT I/F PART
580
SEQUENCER
587
TEST INPUT
COMMAND

FIG. 7


58
TEST INPUT
581
TEST INPUT I/F PART
582
TEST SELECTING PART
583
OUTPUT PART
TEST OUTPUT
56
CONTROLLER MEMORY
570
571
580
SEQUENCER
586
CONTROL FLAG LATCHING CIRCUIT
586
DECODER
584
REGISTER
CIPHER KEY
ACCESS-SIGNAL
LATCH INSTRUCTION

F I G. 8



580
SEQUENCER
5805
REGISTER
STORE-SIGNAL
GENERATING PART
MEMORY
ACCESS-SIGNAL
586
585
584
56
CONTROLLER MEMORY

FIG. 9

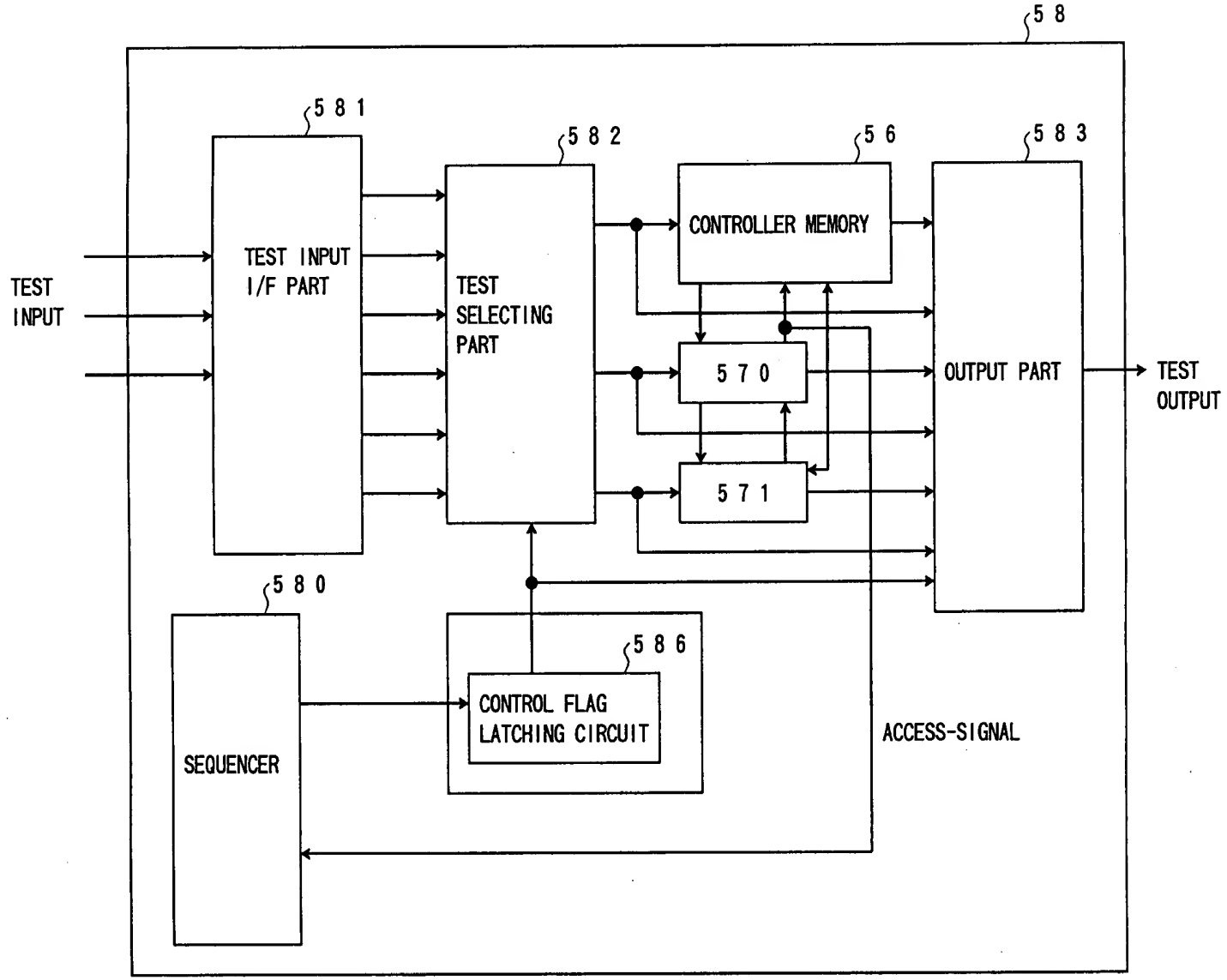

58
581
582
56
583
TEST INPUT I/F PART
TEST SELECTING PART
CONTROLLER MEMORY
OUTPUT PART
TEST INPUT
TEST OUTPUT
570
571
580
586
SEQUENCER
CONTROL FLAG LATCHING CIRCUIT
ACCESS-SIGNAL

FIG. 10A

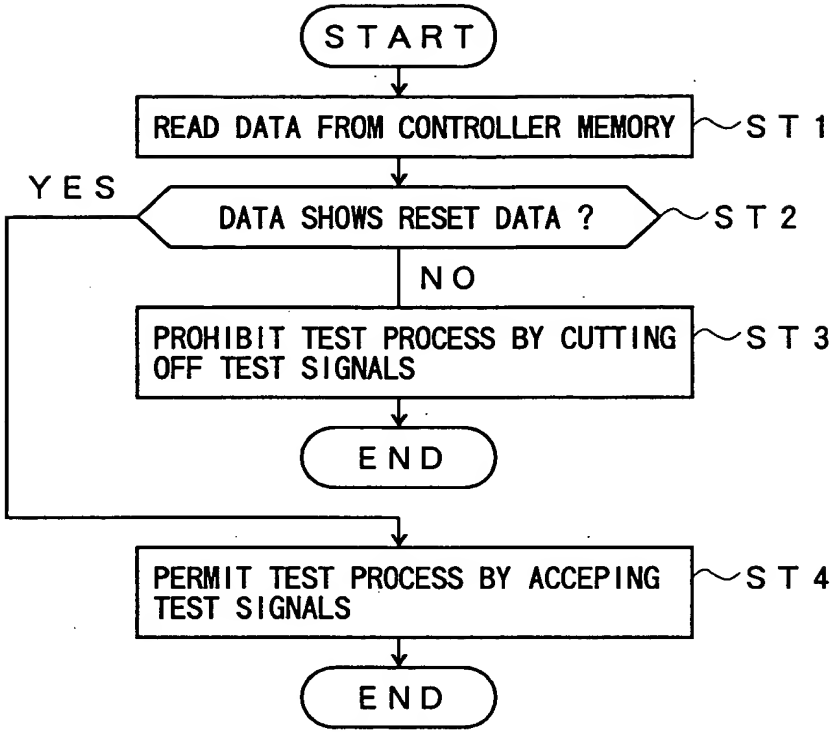


FIG. 10B